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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,258	02/26/2004	Jaime Bayan	NSC1P295/P05886	9477

22434 7590 05/31/2006

BEYER WEAVER & THOMAS LLP
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
DOAN, THERESA T	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/789,258	BAYAN ET AL.	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-7,9-13 and 16-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7,9-13 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 03/14/06 has being acknowledged. By this amendment, claims 1, 8 and 14-15 are cancelled; Claims 2-7, 9-13 and new claims 16-19 are pending in the application.

Claim Objections

2. Claims 17 and 19 are objected to because of the following informalities:

- In claim 17, line 1, a phrase "the peripheral ledges" should be changed to "the recessed ledges" which is mentioned in independent claim 16.
- In claim 19, line 1, a phrase "each of the semiconductor die" should be changed to "each of the semiconductor dies".

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 2-7, 9-13 and 16-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Hasebe et al. (U.S. Pat. 6,713,849) as previously cited.

Regarding claims 2 and 9, Hasebe (Figs. 8 and 18) discloses a substrate panel for use in semiconductor packaging, the substrate panel comprising:

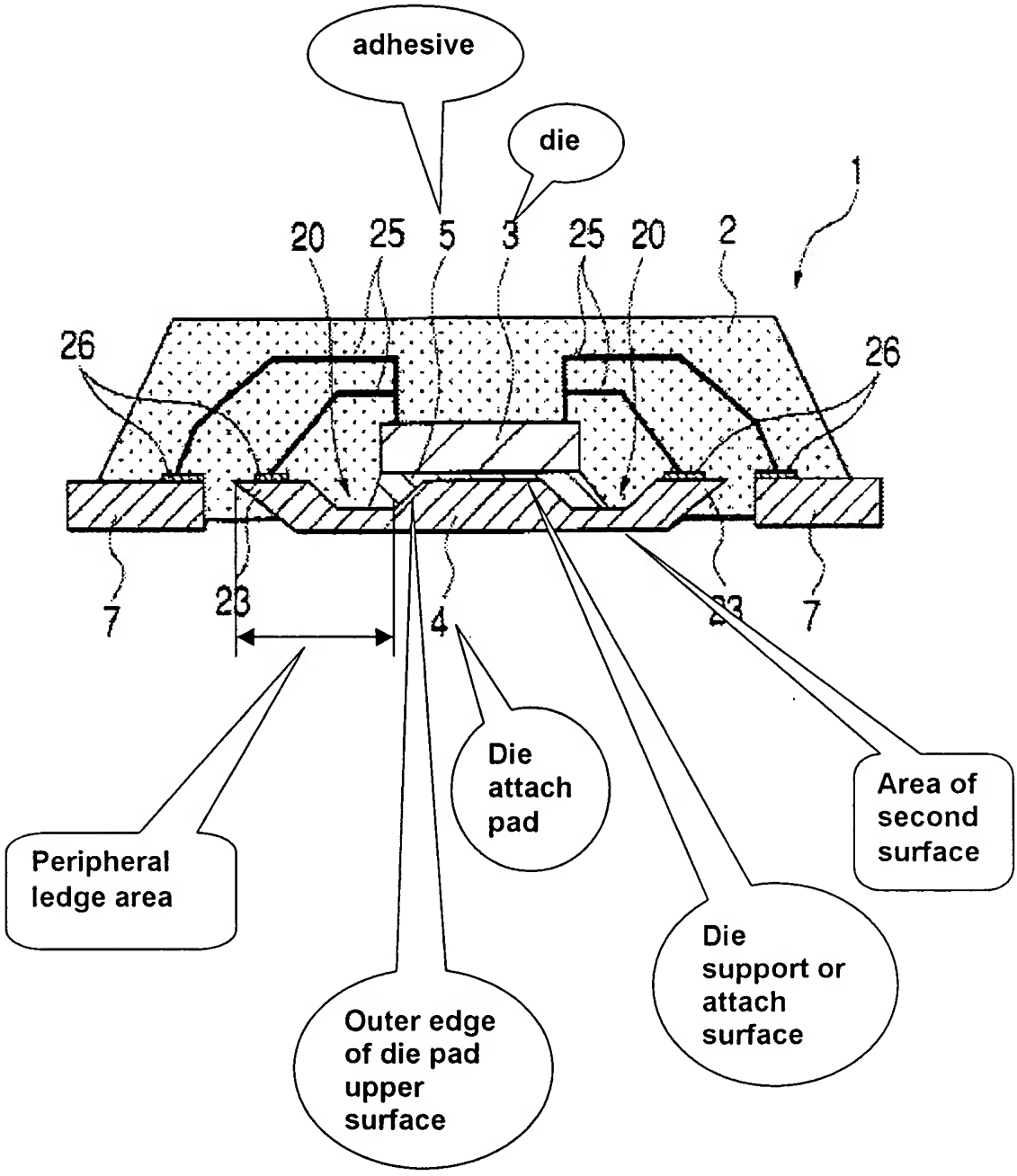
a lead frame panel 40 including a plurality of device areas 41 (Fig. 8, column 10, lines 65-67 and column 11, line 1), each device area 41 having a die attach pad 4 and a plurality of contacts 7, wherein each die attach pad 4 includes a die support surface and a peripheral ledge that is defined as a peripheral portion which extends laterally from the bottom surface of the recess 20 to the tip portion 23 (See Fig. 18 labeled by the examiner below), the peripheral ledge is recessed relative to the die support surface, wherein the peripheral ledges extend around the outer edges of the die attach pads 4; and

a plurality of semiconductor dies (see Fig. 8), each die 3 being attached to the die support surface of an associated die attach pad 4 using an adhesive 5 (Fig. 18 labeled by the examiner below), wherein a portion of each semiconductor die 3 extends beyond an outer edge of its associated die attach pad 4, and wherein the ledge is configured to retain an amount of the adhesive 5 (Fig. 18 labeled by the examiner below and column 12, lines 26-36).

Regarding claim 16, Hasebe (Figs. 8 and 18) discloses a substrate panel for use in semiconductor packaging, the substrate panel comprising:

a lead frame panel 40 including a plurality of device areas 41 (Fig. 8, column 10, lines 65-67 and column 11, line 1), each device area 41 having a plurality of contacts arranged around a die attach pad 4, wherein each die attach pad 4 includes a die support surface and a recessed ledge that is defined as a peripheral portion which extends laterally from the bottom surface of the recess 20 to the tip portion 23 (See Fig. 18 labeled by the examiner below), the recessed ledge has recessed bottom surface 20 being lower than the die support surface and extends along an edge of the die attach pad 4 (also see Fig. 19).

FIG. 18


adhesive
die
1
20
25
5
3
25
20
2
26
26
7
23
4
23
7
Peripheral ledge area
Die attach pad
Outer edge of die pad upper surface
Die support or attach surface
Area of second surface

Regarding claims 3 and 10, Hasebe discloses that each die attach pad 4 has a second surface opposite to the die attach surface, wherein the area of the die attach surface is less than the area of the second surface (See Fig. 18 labeled by the examiner above).

Regarding claims 4 and 11, Hasebe (Fig. 18) discloses that bottom surfaces of the contacts 7 are substantially co-planar with bottom surfaces of the die attach pads 4.

Regarding claims 5 and 12, Hasebe discloses further comprising an encapsulant 2 applied to the lead frame panel 40, wherein the second surfaces of the die attach pads 4 and the bottom surfaces of the contacts 7 are exposed on an outer surface of the encapsulant 2, and wherein the peripheral ledges retain amounts of the adhesive 5 so as to prevent the adhesive from being exposed on the outer surface of the encapsulant 2 (column 12, lines 26-36).

Regarding claims 6 and 13, Hasebe discloses that the semiconductors dies 3 are down bonded to the respective ledges of their associated die attach pads 4 (Fig. 18 labeled by the examiner above).

Regarding claim 7, Hasebe discloses that the lead frame panel 40 comprises a matrix of tie bars 9 arranged in perpendicular rows and columns that define a two dimensional array of the device areas such that adjacent device areas 1 are separated only by the tie bars (Fig. 21 and column 15, lines 35-47).

Regarding claim 17, Hasebe discloses that the peripheral ledge extend entirely around the outer edge of the die attach pads (See Fig. 18 above).

Regarding claim 18, Hasebe discloses that a plurality of semiconductor dies are attached to the die support surface of each die attach pad 4 using an adhesive layer 5, wherein a portion of each semiconductor die 3 extends beyond an outer edge of its associated the die attach pad 4, wherein the ledge is configured to retain an amount of the adhesive 5 (See Fig. 18 above and column 12, lines 26-36).

Regarding claim 19, Hasebe discloses that each of the semiconductor dies 3 are electrically connected with the plurality of contacts 7 arranged around the die 3 and wherein each die 3 and associated electrical connections 25 to the contacts 7 are encapsulated by a resin 2.

Response to Arguments

5. Applicant argues that a groove 20 of Hasebe is not "a peripheral ledge" as claimed (claims 2 and 9) because the groove 20 is interior from the edge of the die attach pad and does not extend to the edge of the die attach pad.

This argument is not persuasive because the groove 20 is not relied on for teaching "a peripheral ledge" as asserted by Applicant, but rather, "a peripheral ledge" in Hasabe's Fig. 18 is defined as a peripheral portion which extends laterally from the bottom surface of the recess 20 to the tip portion 23 (See Fig. 18 labeled by the examiner on page 5). Clearly, the above defined peripheral ledge is formed at outer boundary of the die attach pad and extends to the edge of the die attach pad. Therefore, Fig. 18 of Hasebe does disclose "a peripheral ledge" as claimed in claims 2 and 9.

6. Applicant further argues that Hasebe does not suggest the invention as recited in new claims 16-19.

This argument is not persuasive because Fig. 18 of Hasebe does suggest all the limitations recited in the above new claims, including the limitations of having each die attach pad 4 includes a die support surface and a recessed ledge that is defined as a peripheral portion which extends laterally from the bottom surface of the recess 20 to the tip portion 23, the recessed ledge has recessed bottom surface 20 being lower than the die support surface and extends along an edge of the die attach pad 4 (See ground of refection for more details).

The rest of applicant's arguments have been addressed to the amended claims are considered in the rejections shown above.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Theresa Doan
May 25, 2006.